James Gerald Salisbury

Email: james@salisbury.org.uk

www.salisbury.org.uk

0775 1603010

I am an experienced electronics engineer, and have worked on many complex systems. I have worked as a component support engineer at Altera and have also designed parts of a number of complex digital and mixed signal boards for use at CERN and the Rutherford Appleton Laboratory. I have used a number of different FPGA and CPLD devices from both Xilinx and Altera. I have also designed part of the extension to the timing system on a large physics experiment. I have used VHDL 93, simulated using Modelsim, and PSPICE , and also used Quartus and ISE. I have use labview to read an electricity meter and other items via modbus. I have also used C and a Raspberry PI to read a modbus meter and send the data to a website for display.

Work History

2014 – Present Rockwell Automation LTD

Revising a 16 year old Altera Max Plus II design to using modern VHDL and Microsemi Igloo II parts. Assisting with schematic design and design reviews Capturing design requirements using DOORS. Performing functional decomposition using Visio diagrams.

2012- 2014Radio Detection LTD part of SPX

Implementing safety and reliability into existing products including working to BS61010 and many safety and ESD improvements. This work has included many system and FMEA reviews and working with the Mentor Graphics PADS Logic design suite.

2010 - 2012 Bartington Instruments

Digital design engineer, evaluating the use of 24 bit ADCs to support their instrumentation. I have also evaluated a number of 32 bit microprocessors including the Arm Cortex M0 from NXP and the Microchip PIC 32. Designing a proprietary bus system for readout of the magnetometers over RS485. Entering schematics and carrying out PCB design with Easy PCB software.

2008 – 2009 Altera Europe

Part of Altera's European support team, working on customer board level and FPGA configuration issues. Some of the advice to customers permitted very significant EMC improvements and cost savings

2000 – 2008 Rutherford Appleton Laboratory

Design part of the extension of part of the timing system for ISIS, the world's most powerful pulsed neutron source. This involved design from a high system level down to individual component and firmware, for 3 double eurocard size boards. Target devices on this system were Vertex 4 and Xilinx CPLDs.

The detailed design had to cover areas such as safety, on card power distribution, hot swap, VHDL firmware, backplane & enclosure selection and documentation. I liaised effectively with the onsite PCB drawing office and also enclosure and assembly subcontractors. I had to resolve several technical problems with the enclosures and suggested solutions which I detailed for them to implement.

I have used a number of different software packages, principle ones for firmware design are Libero, HDL Designer, Modelsim, and Quartus. For hardware design I have used Concept HDL, Orcad and PSPICE. I have also used Visio to sketch diagrams and initial layouts.

Previous projects have included selecting and using a Spartan 2E implementing 5 i2c chains, each with several devices, a VME interface and fitting 32, 32 bit wide scalars. Altera CPLDs were used for the front end discriminators. I had to also design the hot swap circuit and suitable filters to enable the use of commercial DC – DC converters. I procured the components for the production run of 63 cards, so had to obtain several quotes and check lead times.

On a different project I had to design the power distribution scheme for a 9U very power hungry VM64X card, and also the ADC input processing.

September 1998 October 2000 DERA Malvern

DERA Graduate engineer, RF communications section. Major tasks, evaluation of radio systems including coordinating a trial on a major system, from test method and equipment selection, obtaining frequency clearances, taking of results and documentation. I also wrote reports on co-location and inter-modulation issues, software radio components also market surveys on the start of the art of RF filters.

Positions of Responsibility

I have performed many parts of the project cycle, planning, suggest the design, evaluate the technical solutions and implement the design I am often asked to evaluate or suggest new test equipment.

Training courses

Advanced VHDL 5 days Doulos
C Programming with TCP-IP Febas
Electrical safety design and CE marking, Keith Armstrong 1 day
Xilinx designing for performance, Doulos
Xilinx tech class, Doulos
Foundation in management excellence.
Comprehensive VHDL 5 day Doulos
Introduction to Xilinx devices 2 day Doulos
Texas instruments industrial data systems seminar, 1 day
Texas instruments power supply design, 1 day.
High speed digital design, 2 Days Howard Johnson,

Education

Swansea University 2009-2010

MSc Electronics Technology for Sustainable Energy, Dissertation 80% Project Matlab, Labview & Smart meters investigating electricity meter fraud. Units included Control, Power Generation, Life Cycle Analysis, Advanced Power Electronics, Wide Band Gap Electronics, Manufacturing systems, Probing at the Nanoscale

Manchester Metropolitan University 1994 -1998

BEng (Hons.) Electrical and Electronic Engineering 2.1 IEE project prize.

Final year units studied; Fibre Optic communications, Power electronics, Microprocessors and Instrumentation. Final year project the design and construction of an RDS receiver.

Hobbies and interests

I have implemented some follow on projects from my Masters, reading an electricity meter over Modbus using a Raspberry PI and then sending the data to a website so the graphs can be seen. I am interested in photography, have visited several countries and taken many interesting photos.

References

References are available on request